1. There is/are error/s in the programs below. Explain the error/s and suggest the correction/s. Sections (a.), (b.), and (c.) are independent of each other.

   a. LEA $6443, A0
      MOVE.L #$0000000010101100, -(A0)  
      (1 mark)

   b. ROR.W #$A,D0  
      (1 mark)

   c. In the program below:

      ![Flowchart](image)

      START

      INPUT DATA

      CLASSIFY DATA AS EVEN OR ODD NUMBER

      MOVE NUMBER TO DATA REGISTER

      END

      PROGRAM

      ORG $400600
      DATA DC.B $03,$B2,$8F,$FA
      DC.B $77,$33,$60,$0C
      START ORG $400400
      LEA DATA,A1
      -----.
      MOVE.B #$9,D4
      INPUT MOVE.B (A1)+,D1
      SUB.B #$1,D4
      CMP.B #$0,D4
      BEQ STOP
      BTST #$0,D1
      BEQ ODD
      BNE EVEN
      -----.
      ODD ROL.L #$8,D3
      ADD.B D1,D3
      BRA INPUT
      EVEN ROL.L #$8,D2
      -----.
      ADD.B D1,D2
      BRA INPUT
      STOP MOVE.B #9,D0
      TRAP #15
      END START  
      (2 marks)

2. An MC68K microprocessor system contains 16kB RAM at base address $100000 and 16kB ROM at base address $500000. Memory devices used are 8k*8bits ROM chips and 8k*8bits RAM chips with 8-bit data lines. Design Partial Address Decoding scheme of the memory system that has been specified above. Please include in your answer script:

   a) The address layout / mapping table to find the lower and upper range of the memory module.

   b) The detailed schematic diagram showing how the memory system is interfaced to the MC68000 using 3 to 8 decoder as shown in Figure Q2 and other necessary logic gates.

   Both EPROM and RAM have $\overline{OE}$ (Output Enable) and $\overline{CS}$ (Chip Select) as control lines. RAM has additional control line called $\overline{WE}$ (Write Enable).

   ![Figure Q2](image)  
   (11 marks)
The circuit in Figure 1 is a simplified version of a top-loading washing machine utilizing MC68000 CPU as its controller. Design a program for washing and spin-dry for the above washing machine. The washing machine should do washing according to the table below.

<table>
<thead>
<tr>
<th>W S</th>
<th>Display</th>
<th>Motor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>O</td>
<td>No operation, motor is locked at North pole</td>
</tr>
<tr>
<td>0 1</td>
<td>S</td>
<td>Spin-dry, motor turns clockwise in high speed for 100 cycle</td>
</tr>
<tr>
<td>1 0</td>
<td>E</td>
<td>Washing, motor turns anti-clockwise and clockwise alternately in moderate speed for 50 cycle</td>
</tr>
<tr>
<td>1 1</td>
<td>L</td>
<td>Emergency stop, motor is lock to stop motor during operation</td>
</tr>
</tbody>
</table>

When both switches are off, motor is locked. When only switch W or S is pressed, operation washing or spin-dry shall commence. During operation, motor can be abruptly stopped by pressing both switches on. At the same time, the 7-segment display shall display O, S, E and L as indication for no operation, spin-dry, washing and emergency stop.

Kindly refer to the diagram and table below for motor operation. An example, to turn motor to the right (north => east) is explained. First, only PB0 is active-High causing north coil to be magnetized while the rest of the poles deactivated. This turns the middle coil of the motor to the north, as indicated by the arrow on the middle coil. Then only turn PB3 to active-High, causing east coil to be magnetized while the rest deactivated. This turns the motor to the right (north => east).
a. Sketch a flowchart for the above system to function as required in the above table.

(5 marks)

b. Translate the flowchart to a 68K CPU assembly language (with comments). Given a 2 delay subroutines as DELAYF for high-speed and DELAYM for moderate-speed, write the delay program and use this subroutine in your program.

(10 marks)

Port initialization is not required.
Program for both delay subroutines are also not required. You are ONLY required to LABEL your subroutine.
Bits 6 and 7 of PORT B are not used.
The display is a common cathode 7-segment display.